Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : STM32G03 and STM32G04 64K - product enhancement

PCN Reference : MDG/22/13306

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STM32G031F4P3	STM32G031K6T6	STM32G031C8T7
STM32G031J6M6	STM32G041F6P6TR	STM32G031K4T6
STM32G031F6P7TR	STM32G030F6P6TR	STM32G031J4M6
STM32G030K6T6	STM32G041K6T6	STM32G031K8T6
STM32G030C8T6	STM32G031K8T3	STM32G030C6T6TR
STM32G041K8T6	STM32G031C8U7	STM32G031C8U6TR
STM32G031K8U7TR	STM32G041F8P6	STM32G031C6U6
STM32G031K4U6	STM32G031F4P6	STM32G031G8U6TR
STM32G041Y8Y6TR	STM32G031K8U7	STM32G031K4U6TR
STM32G031K8T3TR	STM32G031C8U6	STM32G031Y8Y6TR
STM32G041F6P6	STM32G031K8U6TR	STM32G030J6M6
STM32G031F8P6TR	STM32G041J6M6	STM32G031C4U6
STM32G041K8U6	STM32G031F6P6	STM32G031F8P6
STM32G031J6M6TR	STM32G031K8T6TR	STM32G030K6T6TR
STM32G031K8U6	STM32G041G8U6	STM32G031C8T6
STM32G041C8T6	STM32G031C4T6	STM32G031G4U6
STM32G031K6U6	STM32G030F6P6	STM32G041C8U6
STM32G031K4U3	STM32G031G6U6	STM32G041G6U6
STM32G031K4U3TR	STM32G031G8U6	STM32G030K8T6
STM32G031K8T7TR	STM32G030C6T6	STM32G031C6T6
STM32G041C6T6	STM32G031G8U3TR	STM32G031C8U7TR
STM32G030K8T6TR	STM32G031K8T7	STM32G031J6M3
STM32G031G6U6TR	STM32G031G8U3	STM32G031G6U3TR

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PRODUCT/PROCESS CHANGE NOTIFICATION PCN13306 – Additional information

STM32G03 and STM32G04 - product enhancement

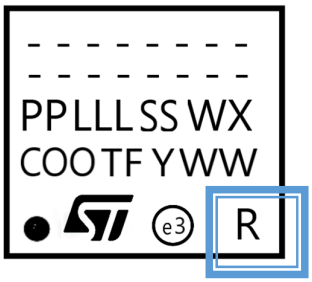
MDG - Microcontrollers Division (MCD)

What are the changes?

Changes described in table below:

STM32G03x STM32G04x	Current Cut1.1	New Cut1.2
Die revision Marking **R**	“Z”	“Y”

Example: Marking on package UFQFPN 7X7X0.55 48L



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- place a **Non-standard** sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number "**PCN13306**" into the NPO Electronic Sheet/**Regional Sheet**
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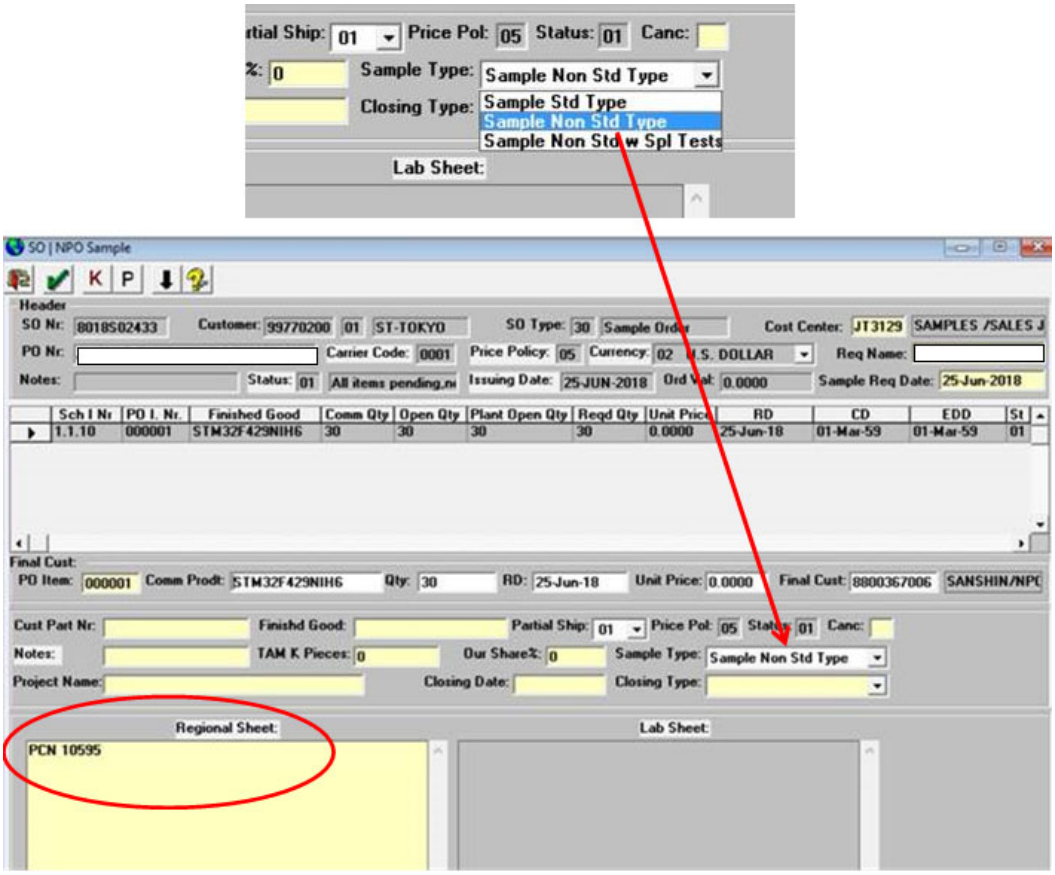

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Reliability Evaluation Report

MDG-MCD-RER1808

STM32G030/G031 / G041x (466x66)

Reliability Evaluation Purpose **(New Product Qualification)**

General Information	
Commercial Product	*STM32G030/G031/G041 x4/x6/x8*
Product Line	466X66
Die revision	466XXXY (Cut1.2)
Product Description	STM32G030/G031/G041x family
Package	LQFP48 7x7, LQFP32 7x7, UQFN48 7x7, UQFN32 5x5, UQFN28 4x4 COL, TSSOP 20 BODY 4.4, SO8N 0.15, WLCSP18
Silicon Technology	: TSMC Fab14 90ULL
Division	: MDG-MCD
Reliability Maturity Level	: *30*

Traceability	
Diffusion Plant	TSMC Fab14, Taiwan
Assembly Plant	JSCC, China STM Shenzhen, China AMKOR ATT1, Taiwan

Reliability Assessment	
Pass	☒
Fail	☐
Investigation required	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Date	Author	Function
1.0	19th-Jun-2019	Berengere ROUTIER-SCAPPUCCI Patrick Aubert	MDG-MCD-Q&R Engineer
1.1	13th Sep-2021	Patrick Aubert	MDG-MCD-Q&R Engineer
2.0	4th Mar-2022	Patrick Aubert	MDG-MCD-Q&R Engineer

APPROVED BY:

V1.0

Function	Location	Name	Date
Division Q&R Manager	Rousset	Frederic BRAVARD	19th-Jun-2019
Division Quality Manager	Rousset	Pascal NARCHE	21th-Jun-2019

V1.1

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	13th Sep-2021

V2.0

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	11th March-2022

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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The aim of this report is to present results of the reliability evaluation performed on STM32G030/G031/G041 x4/x6/x8 – Die 466XXXY

Test vehicle is described here below:

Product	Process or Package	Diffusion or Assembly plant
STM32G031C8T6	90ULL LQFP48 7x7	TSMC Fab14, JSCC
STM32G031K8T6	90ULL LQFP32 7x7	TSMC Fab14, JSCC
STM32G031C8U6	90ULL UQFN48 7x7 0.5	TSMC Fab14, JSCC
STM32G031K8U6	90ULL UQFN32 5x5 0.5	TSMC Fab14, JSCC
STM32G031G8U6	90ULL UQFN28 4x4 COL 0.5	TSMC Fab14, JSCC
STM32G031F8P6	90ULL TSSOP 20 BODY 4.4 0.65	TSMC Fab14, STM Shenzhen
STM32G031J6M6	90ULL SO8N 0.15 JEDEC	TSMC Fab14, STM Shenzhen
STM32G031Y8Y6TR	90ULL WLCSP18	TSMC Fab14, ATT1

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard

1.2 Reliability Strategy

The STM32G030/G031/G041 x4/x6/x8 – Die 466XXXZ – is processed in the 90ULL process from TSMC Fab14 Taiwan plant which is qualified since 2014 through STM32L4 – Die 415 (RERMCD1112) for our division.
It is a derivate version of the STM32G071x – 128K – Die 460 (RERMCD1602)

All packages used for the STM32G030/G031/G041x – Die 466XXXZ are qualified at division level.

Package	Reference	Assy Plant location
LQFP 7x7 48L	RERMCD1621	JSCC, China
LQFP 7x7 32L	RERMCD1621	JSCC, China
UQFN 7x7 48L	RERMCD1622	JSCC, China
UQFN 5X5 32L	RERMCD1622	JSCC, China
UQFN 4x4 COL 28L	RERMCD1623	JSCC, China
TSSOP 20L	RERMCD1039	STM Shenzhen, China
SO8N 0.15	RERMCD1708	STM Shenzhen, China
WLCSP18 P0.4	RERMCD1112	ATT1, Taiwan

Based on these data, and according to "RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION" specification (DMS 0061692), the following qualification strategy has been defined:

- Die Qualification:
  - Cut1.0: Full qualification lot to assess the die in LQFP48 package
  - Cut1.1: Subset qualification lot to assess the die in LQFP48 package, including additional HBM characterization allowing to grant 2kV pass
  - Cut 1.2 : Subset qualification lot to assess design fixes in LQFP48 package

- Package Qualification:
  - The reliability test plan and result summary are presented in the following tables:

Package	Body	Pitch	Package Code	Wire	Assy	Trial
LQFP48	7x7	0.5	5B	Silver	JSCC	1 reliability lot
LQFP32	7x7	0.5	5V	Silver	JSCC	CDM
UQFN48	7x7	0.5	MI	Silver	JSCC	1 reliability lot
UQFN32	5X5	0.5	MG	Silver	JSCC	CDM
UQFN28	4x4	0.5	MB	Gold	JSCC	1 reliability lot
TSSOP 20	-	0.65	YA	Silver	STM Shenzhen	1 reliability lot
SO8N	-	1.27	O7	Gold	STM Shenzhen	1 reliability lot
WLCSP18	-	0.4	J3	-	ATT1	1 reliability lot

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for the STM32G030/G031/G041 x4/x6/x8 – Die 466XXXY in all packages listed in the Chapter 1.2.

Refer to Section 3.0 for reliability test results.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1 Generalities

The STM32G031x4/x6/x8 mainstream microcontrollers are based on high-performance Arm® Cortex®-M0+ 32-bit RISC core operating at up to 64 MHz frequency. Offering a high level of integration, they are suitable for a wide range of applications in consumer, industrial and appliance domains and ready for the Internet of Things (IoT) solutions. The devices incorporate a memory protection unit (MPU), high-speed embedded memories (up to 64 Kbytes of Flash program memory and 8 Kbytes of SRAM), DMA and an extensive range of system functions, enhanced I/Os and peripherals

For additional information concerning the product behaviour, refer to STM32G031x4/x6/x8 datasheet.

2.2 Traceability

2.2.1 Wafer fab information

Table 1

Wafer fab information	
FAB1	
Wafer fab name / location	TSMC Fab14 / Taiwan
Wafer diameter (inches)	12 inch
Wafer thickness (µm)	775µm +/- 25µm
Silicon process technology	TSMC090 ULL
Number of masks	45
Die finishing front side (passivation) materials/thicknesses	FSG + NITRIDE 1um
Die finishing back side Materials/thicknesses	NA
Die area (Stepping die size) (µm)	X=1889.6 Y=2165.6
Die pad size (µm)	123, 59
Sawing street width (X,Y) (µm)	80, 80
Metal levels/Materials/Thicknesses (µm)	Rank - Metal composition - Thickness (um) 1 - TaN/Ta/CuSeed/Cu - 0.240 / 2 - TaN/Ta/CuSeed/Cu - 0.310 3 - TaN/Ta/CuSeed/Cu - 0.310 / 4 - TaN/Ta/CuSeed/Cu - 0.310 5 - TaN/Ta/CuSeed/Cu - 0.310 / 6 - TaN/Ta/CuSeed/Cu - 0.850 7 - AlCu - 1.450
Die over coating (material/thickness)	NA
FIT level (Ea=0.7eV, C.L: 60%, 55°C)	2.3 FITs at qualification date
Soft Error Rate - Alpha SER [FIT/Mb] - Neutron SER [FIT/Mb] - Conditions	Alpha SER: 491 FIT/Mb Neutron SER: 445 FIT/Mb Neutron SER is an estimation at sea level of NYC (14n/h/cm²). Alpha result is estimated using a nominal flux of 0.001α/h/cm²
Wafer Level Reliability - Electro-Migration (EM) - Time Dependent Dielectric Breakdown (TDDB) or Gate Oxide Integrity (GOI) - Hot Carrier Injection (HCI) - Negative Bias Thermal Instability (NBTI) - Stress Migration (SM)	Yes
Other Device(s) using same process	STM32L4x/G0x 415, 435, 460, 461, 462, 464, 468, 470

2.2.2 Assembly information

Table 2

Assembly Information	
Package 1 – LQFP 48 7x7x1.4 1 | 5B	
Assembly plant name / location	Statschippac Semi-conductor Jiangyin Co., Ltd. Jiangsu 214437 China
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375+/-25
Die sawing method	Mechanical dicing
Lead frame/Substrate material/supplier/reference	LQFP48L 210sq no slots STMP LF JSCC
Die attach material/type(glue/film)/supplier	Ablestik 3230
Wire bonding material/diameter/supplier	Ag 96.5 0.8 MIL Diam
Molding compound material/supplier/reference	Sumitomo low alpha G631SHQ
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 2 - LQFP 32 7x7x1.4 1 | 5V	
Assembly plant name / location	Statschippac Semi-conductor Jiangyin Co., Ltd. Jiangsu 214437 China
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375+/-25
Die sawing method	Mechanical dicing
Lead frame/Substrate material/supplier/reference	LQFP32L 210sq no slots STMP LF JSCC
Die attach material/type(glue/film)/supplier	Ablestik 3230
Wire bonding material/diameter/supplier	Ag 96.5 0.8 MIL Diam
Molding compound material/supplier/reference	Sumitomo low alpha G631SHQ
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 3 - UFQFPN 7X7X0.55 48L 0.5 MM PITCH|A0B9	
Assembly plant name / location	Statschippac Semi-conductor Jiangyin Co., Ltd. Jiangsu 214437 China
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150 +/- 25
Die sawing method	Mechanical dicing
Lead frame/Substrate material/supplier/reference	LF FOR UQFN 7x7 48L Sn PAD 5.2 MM SQ Groove
Die attach material/type(glue/film)/supplier	GLUE ABLEBOND 8290
Wire bonding material/diameter/supplier	Ag 96.5 / 0.8 MIL
Molding compound material/supplier/reference	RESIN SUMITOMO G770
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3

Package 4 - UFQFPN 5X5X0.55 32L 0.5 MM PITCH|A0B8	
Assembly plant name / location	Statschippac Semi-conductor Jiangyin Co., Ltd. Jiangsu 214437 China
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150 +/- 25
Die sawing method	Mechanical dicing
Lead frame/Substrate material/supplier/reference	LF FOR UQFN 5x5 32L Sn PAD 3.1 MM SQ Groove
Die attach material/type(glue/film)/supplier	GLUE ABLEBOND 8290
Wire bonding material/diameter/supplier	Ag 96.5 / 0.8 MIL
Molding compound material/supplier/reference	RESIN SUMITOMO G770
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 5 - UFQFPN 4X4X0.55 28L PITCH0.5 COL|A0B0	
Assembly plant name / location	Statschippac Semi-conductor Jiangyin Co., Ltd. Jiangsu 214437 China
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150 +/- 25
Die sawing method	Mechanical dicing
Lead frame/Substrate material/supplier/reference	Rough mic PPF LF UQFN4x4 COL JSCC
Lead frame finishing (material/thickness)	NiPdAu
Die attach material/type(glue/film)/supplier	DAF HITACHI HR-5104
Wire bonding material/diameter/supplier	GOLD / 0.8 MIL
Molding compound material/supplier/reference	SUMITOMO EME G770HCD
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 6 - TSSOP 20 BODY 4.4 PITCH 0.65 | YA	
Assembly plant name / location	Shenzen STS Microelectronics co.,Ltd 16, Tao Hua Rd. Futian Free Trade Zone Shenzhen, P.R. China 518048
Pitch (mm)	0.65
Die thickness after back-grinding (µm)	280 +/- 20
Die sawing method	Laser Grooving + Mechanical dicing
Lead frame/Substrate material/supplier/reference	FRAME TSSOP 20L 3x4.20 HDMt OpB NiPdAuET
Die attach material/type(glue/film)/supplier	GLUE LOCTITE ABLESTIK 8601S-25
Wire bonding material/diameter	WIRE Ag 96.5% D0.8 BL>5.5 EL2-12 1000m
Molding compound material/supplier/reference	RESIN SUMITOMO EME-G700KC D14mm W4.8g
Package Moisture Sensitivity Level (JEDEC J-STD020D)	1

Package 7 - SO 08 .15 JEDEC | O7	
Assembly plant name / location	Shenzhen
Pitch (mm)	1.27
Die thickness after back-grinding (µm)	280 +/- 20
Die sawing method	Laser Grooving + Mechanical dicing
Lead frame/Substrate material/supplier/reference	FRAME SO 8L 95x130 SHD OpR DP 4Layers
Die attach material/type(glue/film)/supplier	GLUE LOCTITE ABLESTIK 8601S-25
Wire bonding material/diameter	GOLD / 0.8 MIL
Molding compound material/supplier/reference	RESIN SUMITOMO EME-G700KC D16mm W10.2g
Package Moisture Sensitivity Level (JEDEC J-STD020D)	1
Package 8 WLCSP 18L P 0.4 DIE 466 | B06E	
Assembly plant name / location	AMKOR TAIWAN HSINCHU 303 / TAIWAN R.O.C
Pitch (mm)	0.4
Die thickness after back-grinding (µm)	355µm +/- 25µm
Die sawing method	Laser grooving + mechanical dicing
Balls metallurgy/diameter/supplier (BGA/CSP)	Solder ball SAC405 Diam. 230µm
Routing/Redistribution layer (RDL) material (CSP)	RDL Copper 6um
PBO passivation material (CSP)	HD8820
Backside coating material/thickness (CSP)	Back side coating PET film
Molding compound material/supplier/reference	NA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	1

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 4

Lot #	Diffusion Lot	Die Revision (Cut)	Trace Code / Assy Lot	Raw Line	Package	Note
1	9R819111	1.0	GQ84624Z	S15B*466ESXA	LQFP48	Die & Package qual
2	9R819111	1.0	GQ846260	S15V*466ESXA	LQFP32	Package qual
3	9R830026	1.0	GQ849272	S1MI*466ESXA	UQFN 48	Package qual
4	9R830026	1.0	GQ8482AQ	S1MG*466ESXA	UQFN 32	Package qual
5	9R830026	1.0	GQ8482AN	S1MB*466ESXA	UQFN 28	Package qual
6	9R820157	1.0	GK90101U / GK90101U02	C1YA*466ESXA	TSSOP 20	Package qual
7	9R830026	1.0	GK90101U / GK90101U01	C0O7*466ESXA	SO 8	Package qual
8	9R830026	1.0	A585100T	T1J3*466ESXA	WLCSP18	Chipboard assy
9	9R842065	1.1	GQ91525M	S15B*466ESXZ	LQFP48	Die qual
10	9R842065	1.1	GQ91525M	S15B*466XXXZ	LQFP48	Die qual
11	9R110395	1.2	GQ2012BH	705B*466ESXY	LQFP48	Die qual

3.2 Test plan and results summary

Table 5 – ACCELERATED LIFETIME SIMULATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	Ta=125°C Duration= 168h/1200H 3V6	2	77	154	Lot1: 1200h 0/77 Lot9: 168h 0/77 Lot11: 168h 0/77	N/A
ESD HBM	ANSI/ESDA/ JEDEC JS-001	1500 Ω, 100 pF	2	3	6	Lot1 : 0/3 1kV class 1C Lot10: 0/3 2kV class 2 Lot11: 0/3 2kV class 2	N/A
LatchUp	JESD78	130°C	2	3	6	Lot1: 0/3 Lot9: 0/3 Lot11: 0/3	N/A
EDR	JESD22-A117	10kcy EW @ 125°C then Storage HTB 150°C – 168h / 1500H	2	77	154	Lot1: 1500h 0/77 Lot9: 168h 0/77	N/A
EDR	JESD22-A117	10kcy EW @ 25°C then Storage HTB 150°C – 168h	2	77	154	Lot1: 0/77 Lot9: 0/77	N/A
EDR	JESD22-A117	10kcy EW @ -40°C then Storage HTB 150°C – 168H	2	77	154	Lot1: 0/77 Lot9: 0/77	N/A
ELFR	JESD22-A108 JESD74	Ta=125°C Duration= 48hrs 3V6	1	500	500	Lot1: 0/500	N/A

Table 6 – ACCELERATED ENVIRONMENT STRESS TESTS

For LQFP7x7 48L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V Class C2a	1	3	3	Lot1: 0/3 Lot11: 0/3	N/A
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot1: 0/308	N/A
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot1: 0/77	N/A
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot1: 0/77	N/A
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	1	77	77	Lot1: 0/77	N/A
THB	JESD 22-A101	Ta=85°C/85%RH Duration= 1000hrs VDD=3v6 ☒ After PC	1	77	77	Lot1: 0/77	N/A

For LQFP7x7 32L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V Class C2a	1	3	3	Lot2: 0/3	

For UQFN7x7 48L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V Class C2a	1	3	3	Lot3: 0/3	N/A
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot3: 0/308	N/A
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot3: 0/77	N/A
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot3: 0/77	N/A
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	1	77	77	Lot3: 0/77	N/A
THB	JESD 22-A101	Ta=85°C/85%RH Duration= 1000hrs VDD=3v6 ☒ After PC	1	77	77	Lot3: 0/77	N/A

For UQFN5x5 32L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V Class C2a	1	3	3	Lot4: 0/3	N/A

For UQFN4x4 28L COL, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V Class C2a	1	3	3	Lot5: 0/3	N/A
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot5: 0/308	N/A
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot5: 0/77	N/A
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot5: 0/77	N/A
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	1	77	77	Lot5: 0/77	N/A
THB	JESD 22-A101	Ta=85°C/85%RH Duration= 1000hrs VDD=3v6 ☒ After PC	1	77	77	Lot5: 0/77	N/A

For TSSOP 20L, STM Shenzhen

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V Class C2a	1	3	3	Lot6: 0/3	N/A
PC	J-STD-020	24h bake@125°C, MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot6: 0/308	N/A
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot6: 0/77	N/A
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot6: 0/77	N/A
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	1	77	77	Lot6: 0/77	N/A
THB	JESD 22-A101	Ta=85°C/85%RH Duration= 1000hrs VDD=3v6 ☒ After PC	1	77	77	Lot6: 0/77	N/A

For SO8N 0.15, STM Shenzhen

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V Class C2a	1	3	3	Lot7: 0/3	N/A
PC	J-STD-020	24h bake@125°C, MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot7: 0/308	N/A
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot7: 0/77	N/A
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot7: 0/77	N/A
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	1	77	77	Lot7: 0/77	N/A
HAST	JESD 22-A110	Ta=110°C ,85% RH Duration= 264h VDD=3v6 ☒ After PC	1	77	77	Lot7 : 0/77	N/A

For WLCSP18, ATT1

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V Class C2a	1	3	3	Lot8: 0/3	N/A
PC	J-STD-020	24h bake@125°C, MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot8: 0/308	WLCSP18 mounted on chipboard
TC	JESD22-A104	Ta=-40/125°C Duration= 850cyc (1) ☒ After PC	1	77	77	Lot8: 0/77	WLCSP18 mounted on chipboard
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot8: 0/77	WLCSP18 mounted on chipboard
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	1	77	77	Lot8: 0/77	WLCSP18 mounted on chipboard
THB	JESD 22-A101	Ta=85°C/85%RH Duration= 1000hrs VDD=3v6 ☒ After PC	1	77	77	Lot8: 0/77	WLCSP18 mounted on chipboard

Note (1): Reliability condition adapted for WLCSP18 mounted on chipboard

Table 7 – PACKAGE ASSEMBLY INTEGRITY TESTS

For TSSOP 20

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis	Internal ST specifications	1	50	150	Lot6: 0/50	N/A

For SO8N

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis	Internal ST specifications	1	50	50	Lot7: 0/50	N/A

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
ANSI/ESDA JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
ANSI/ESDA JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD78	IC Latch-up test
JESD 22-A108	Temperature, Bias and Operating Life
JESD 22-A117	Endurance and Data retention
JESD 22-A103	High Temperature Storage Life
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104:	Temperature cycling
JESD22-A110:	Biased Highly Accelerated temperature & humidity stress
JESD22-A101:	Temperature Humidity Bias
JESD 22B102:	Solderability test
JESD22B100/B108:	Physical dimension

5 GLOSSARY

Reference	Short description
HTOL	High Temperature Operating Life
EDR	Endurance and Data Retention
ELFR	Early Failure Rate
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HAST	Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD HBM	Electrostatic discharge (human body model)
ESD CDM	Electrostatic discharge (charge device model)
LU	Latch-up
CA	Construction Analysis

6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1	Patrick AUBERT Berengere ROUTIER-SCAPPUCCI	Initial version	MDG-MCD-Q&R Engineer	Rousset	Frederic BRAVARD	19th June 2019
					Pascal NARCHE	21 rst June 2019
1.1	Patrick AUBERT	Complementary HBM (lot10)	MDG-MCD-Q&R Engineer	Grenoble	Dominique Galiano	13th Sep 2021
2	Patrick AUBERT	Cut 1.2 results	MDG-MCD-Q&R Engineer	Rousset	Dominique Galiano	11th March 2022

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